Abstract

Digital Signal Processors (DSP) are real-time computing devices that are significant component in today’s advanced technological life. From personal computers to digital cameras, from mobile phones to configurable home appliances, DSPs work as the brain to the specific tasks, that is ordered to be performed by electronic devices. Like personal computer’s processors, DSPs are also being modified regularly to provide improved functionality of electronic devices with respect to their portability, power consumption and better performances.

One of the key players in manufacturing DSPs is Texas Instruments (TI), a Dallas based microchip producers in the United States.

This report is based on TI’s C6000 DSP series the TMS320C6416 microprocessor. More specifically this report is to briefly enlighten the Very Long Instruction Word (VLIW) instruction architecture that TMS320C6416 is based on. Some technical aspects of C6416 core have also been explained with in this report with TI’s documentation support.

This report is being produces as an assignment under MSc. Program of Electrical Engineering at Frederick Institute of Technology under the supervision of Mr. Konstantinos Tatas.
# Table of Contents

Abstract ..................................................................................................................... 1
Table of Contents ...................................................................................................... 2
Chapter 1: Introduction .......................................................................................... 3
1.1 Digital Signal Processor .................................................................................. 3
1.2 Very Large Instruction Word (VLIW) .......................................................... 4
Chapter 2: TMS320C6416 DSP .......................................................................... 6
2.1 TMS320C6416 Overview ............................................................................... 6
2.1.1 Co-Processors ......................................................................................... 6
2.1.2 Cache Memory ......................................................................................... 6
2.1.3 Complete Characteristics Table of C64x DSP ........................................ 7
2.2 DSP Core ....................................................................................................... 8
2.2.1 Instruction Architecture ......................................................................... 8
2.2.2 Load/Store Architecture ......................................................................... 8
2.2.3 Arithmetic Operations ............................................................................ 10
Chapter 3: Supports and Applications ................................................................. 11
3.1 Peripheral Support ....................................................................................... 11
3.2 Development Tools ..................................................................................... 12
3.2.1 Software Development Tools ............................................................... 12
3.2.2 Hardware Development Tools ............................................................... 12
3.3.3 Applications ......................................................................................... 12
References ........................................................................................................... 13
Appendix ............................................................................................................... 14
Chapter 1: Introduction

This chapter will explain the behaviours of DSPs (Digital Signal Processors) and VLIW (Very Long Instruction Word).

1.1 Digital Signal Processor (DSP)

A DSP is real-time computing microprocessor that is specifically designed for signal processing. Although general purpose processors can be used for digital signal processing but a dedicated DSP contains architectural optimizations for faster processing. Moreover they are designed as cost, power and heat effective devices.

Some general characteristics of DSPs are:

a) Real-time computing device.

b) Uses ADC and DAC for signal processing.

c) Based on Harvard Architecture.

Other features have also been introduced in advanced DSPs that are becoming part of the design, such as individually handling multitasking without any hardware support, separate instructions for SIMD operations etc. Generally, in embedded micro-controllers such as ASIC, FPGA, Configurable etc. DSPs have been the most efficient in almost every aspect that comes into consideration. The following tables are extracted from Taxes Instruments White Paper that shows what aspects have been considered while comparing microprocessors and how the different microprocessors performed within those aspects.
1.2 Very Large Instruction Word (VLIW)

VLIW is a microprocessor architecture in which a compiler divides application instructions into basic operations that a processor can easily perform in parallel, the technique also referred to as Instruction Level Parallelism (ILP). The operations are placed in very long instruction word, which a processor can break accordingly without any further analysis in order to handle them individually.

VLIW processing scheme is known as superscalar in which multiple instructions are executed in parallel based on fixed routine of code compilation, which is a step further from pipelining scheme where parts of instructions are executed in parallel.

VLIW instructions are 64-bit wide or more, unlike the other superscalar CPUs which rather have greater number of ALUs to execute operations in parallel, because each VLIW instruction performs multiple operations per cycle. In VLIW processors, scheduling of operations execution is handled by compiler.
The most significant hardware related advantage of VLIW processors are that the compilers have to handle the order of operations and their executions, thus processors does not carry logical burden regarding of all the resources are used in computation rather than being shared with branch estimation, determining the order of instructions’ execution. This approach has also made VLIW processors rather simpler than other superscalar CPUs.
Chapter 2: TMS320C6416 DSP

2.1 TMS320C6416 Overview

A production of Taxes Instruments under its C6000 DSP series, TMS320C6416 is among the highest performance fixed-point digital processors based on TI’s invention VelociTI.2 that is VLIW core architecture. It consists on six ALUs from 32 to 40 bit. Each ALU supports single 32-bit, dual 16-bit or quad 8-bit arithmetic operations per clock cycle. It has 64 32-bit general purpose registers. With the rate of performing 5760 MIPS at 720 MHz clock speed, the device presents low cost tool against high performance DSP programming challenges. C6416 is capable of producing four 16-bit Multiply Accumulates (MACs) per cycle for a total of 2880 million MACs per second (MMACS).

2.1.1 Co-processors

C6416 device has a couple of high performance integrated co-processors names Viterbi Decoder coProcessor (VDP) and Turbo Decoder coprocessor (TCP), which significantly boost up on-chip channel decoding tasks.

2.1.2 Cache Memory

A TMS320C6416 has two levels of cache memories. The L1 program cache (L1P) is a 128-Kbit direct mapped cache and the L1 data cache (L1D) is also 128-Kbit but uses 2 way set associative approach. The L2 cache consists of an 8-Mb memory space that is mutual for program and data.
### 2.1.3 Complete Characteristics Table of C64x DSP

<table>
<thead>
<tr>
<th>HARDWARE FEATURES</th>
<th>C6414, C6415, AND C6416</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Peripherals</strong></td>
<td></td>
</tr>
<tr>
<td>EMIFA (64-bit bus width) (default clock source = AECLKIN)</td>
<td>1</td>
</tr>
<tr>
<td>EMIFB (16-bit bus width) (default clock source = BECLKIN)</td>
<td>1</td>
</tr>
<tr>
<td>EDMA (64 independent channels)</td>
<td>1</td>
</tr>
<tr>
<td>HPI (32- or 18-bit user selectable)</td>
<td>1 (HPI16 or HPI32)</td>
</tr>
<tr>
<td>PCI (32-bit [DeviceID Register value 0xA10E])</td>
<td>1 [C6415/C6416 only]</td>
</tr>
<tr>
<td>McBSPs (default internal clock source = CPU/4 clock frequency)</td>
<td>3</td>
</tr>
<tr>
<td>UTOPIA (8-bit mode)</td>
<td>1 [C6415/C6416 only]</td>
</tr>
<tr>
<td><strong>Peripheral performance is dependent on chip-level configuration.</strong></td>
<td></td>
</tr>
<tr>
<td>32-Bit Timers (default internal clock source = CPU/8 clock frequency)</td>
<td>3</td>
</tr>
<tr>
<td>General-Purpose Input/Output 0 (GPIO)</td>
<td>18</td>
</tr>
<tr>
<td><strong>Decoder Coprocessors</strong></td>
<td>1 (C6416 only)</td>
</tr>
<tr>
<td>VCP</td>
<td>1 (C6416 only)</td>
</tr>
<tr>
<td>TCP</td>
<td>1 (C6416 only)</td>
</tr>
<tr>
<td><strong>On-Chip Memory</strong></td>
<td>1024K</td>
</tr>
<tr>
<td>Size (Bytes)</td>
<td>16K-Byte (16KB) L1 Program (L1P) Cache</td>
</tr>
<tr>
<td>Organization</td>
<td>16KB L1 Data (L1D) Cache</td>
</tr>
<tr>
<td>Control Status Register (CSR[31:16])</td>
<td>1024KB Unified Mapped RAM/Cache (L2)</td>
</tr>
<tr>
<td>CPU ID + CPU Rev ID</td>
<td>0x0001</td>
</tr>
<tr>
<td><strong>Device_ID</strong></td>
<td>1024K</td>
</tr>
<tr>
<td>Silicon Revision Identification Register (DEVICE_REV[19:10])</td>
<td>DEVICE_REV[19:10]</td>
</tr>
<tr>
<td>Address: 0x01B0 0200</td>
<td>1.03 or earlier</td>
</tr>
<tr>
<td>1111</td>
<td>1.03</td>
</tr>
<tr>
<td>0001</td>
<td>1.1</td>
</tr>
<tr>
<td>0010 or 0000</td>
<td>2.0</td>
</tr>
<tr>
<td>0011</td>
<td>2.0</td>
</tr>
<tr>
<td><strong>Frequency</strong></td>
<td>500, 600, 720</td>
</tr>
<tr>
<td><strong>Cycle Time</strong></td>
<td>ns</td>
</tr>
<tr>
<td>2 ns (C6414-SE0, C6415-SE0, C6416-SE0) and (C6414A-SE0, C6415A-SE0, C6416A-SE0)</td>
<td>1.87 ns (C6414-SE3, C6415-SE3, C6416-SE3) and (C6414A-SE3, C6415A-SE3, C6416A-SE3)</td>
</tr>
<tr>
<td>[500-MHz CPU, 100-MHz EMIF]</td>
<td>[800-MHz CPU, 133-MHz EMIF] [720-MHz CPU, 133-MHz EMIF]</td>
</tr>
<tr>
<td>1.39 ns (C6414-7E3, C6415-7E3, C6416-7E3)</td>
<td></td>
</tr>
<tr>
<td><strong>Voltage</strong></td>
<td>1.2 V (5SE0)</td>
</tr>
<tr>
<td>Core (V)</td>
<td>1.25 V (A-SE0)</td>
</tr>
<tr>
<td>1.4 V (B-SE3, A-SE3, -SE2)</td>
<td>3.3 V</td>
</tr>
<tr>
<td>I/O (V)</td>
<td>Bypass (x1), x6, x12</td>
</tr>
<tr>
<td>PLL Options</td>
<td>832-Pin BGA (GLZ, ZLZ and CLZ)</td>
</tr>
<tr>
<td>BGA Package</td>
<td>0.13 μm</td>
</tr>
<tr>
<td>Process Technology</td>
<td>0.13 μm</td>
</tr>
<tr>
<td>Product Status</td>
<td>Product Preview (PP), Advance Information (AI), Production Data (PD)</td>
</tr>
</tbody>
</table>

Fig. 3 Characteristics of C64x
2.2 DSP Core

C6416 CPU has two sets of functional units where each set consist of four units and one register file. One set contains functional units named .L1, .S1, .M1 and .D1 where as the other set holds .D2, .M2, .S2, .L2. The two register files in each functional unit contain 32 numbers of register, each register is 32-bit wide.

2.2.1 Instruction Architecture

C6416 instructions are 256-bit wide, known as VelociTI.2. The CPU fetches these instructions words and distributes them in up to eight 32-bit instructions for eight functional units in each clock cycle. The VelociTI architecture handles the instructions supply to eight functional units, if any unit is busy, it will not get any instruction until it’s available.

The first bit of 32-bit instruction decides whether the next instruction belongs to the last executed operation or it should be executed as part of the next execution operation in the following cycle. The fetch instructions are always 256-bit in width however execute instructions can differ in their widths. The variable length execute instruction is one of the most important memory saving feature of C64x CPUs that makes it different from other VLIW processors.

2.2.2 Load/Store Architecture

Another key feature of C64x CPU is its load/store architecture. All the instructions uses operate on registers rather than data memory with the help of two sets of data addressing units named .D1 and .D2. Both .D units are responsible for all data transfer between register files and memory. The data address processed by .D units enables data addresses generated from one register file to the other in order to be used for data load or storage. The .D units have capability of loading and storing a byte, half a word, a word and a double-word in a single instruction.*

* Byte = 8-bits, half a word = 16-bits, a word = 32-bits, double-word = 64-bits
Fig. 4 CPU core block diagram
2.2.3 Arithmetic Operations

There are a couple of special functional units for multiplication operations in C64x CPU called .M. Each .M unit can perform 16 x 16 or 8 x 8 bit multiplies per clock cycle. The .M unit can also perform 16 x 32 bit operations, dual 16 x 16 bit multipliers with add and subtract operations and quad 8 x 8 bit multiplies with add operations. .M units are also capable of bidirectional shift operations.

There are two more functional units called .S and .L. These are for generic arithmetic, logic and branch operations. The AL functions on C64x CPU include single 32-bit, dual 16-bit and quad 8-bit operations.
Chapter 3: Supports and Applications

This chapter will cover the peripherals and applications that are related to C64x CPU. Also there will be some discussion about the development tools provided by Taxes Instruments.

3.1 Peripheral Support

C64x has state-of-the-art compatibility with peripheral devices. The list of supported peripherals is as follows:

2.2.3a. Enhanced Direct Memory Access (EDMA) Controller
2.2.3b. Peripheral Component Interconnect (PCI)
2.2.3c. Universal Test and Operation PHY Interface for ATM (UTOPIA)
2.2.3d. Viterbi Coprocessor (VCP)
2.2.3e. Turbo Coprocessor (TCP)
2.2.3f. External Memory Interfaces (EMIFs)
2.2.3g. Multi-channel Buffered Serial Ports (McBSPs)
2.2.3h. Host Port Interfaces (HPI)
2.2.3i. Direct Memory Access (DMA) Controller
2.2.3j. 32-bit Expansion Bus ("X-Bus")
2.2.3k. Rapid IO™

Each aforementioned names have brief explanation in appendix at the end of this report.
3.2 Development Tools

Texas Instruments has an extensive line of development tools for C6000 DSP platform. The tools provide features such as performance monitoring, code generation, implementations of developed algorithms and fully integrated debug software and hardware modules.

The following products support development of C6000 DSP based applications:

3.2.1 Software Development Tools

a) Code Composer Studio IDE.
b) C/C++/Assembly code generation and debugging development tools
c) Scalable, Real-Time foundation software (DSP/BIOS) that provides the basic run-time target software needed to support any DSP application.

Texas Instruments also have Free Evaluation Tools (FETs) that can be downloaded from their website http://focus.ti.com or a CD can be requested.

3.2.2 Hardware Development Tools

Extended Development System (XDS) Emulator (supports C6000 DSP multiprocessor system debug) EVM (Evaluation Module).

3.3 Applications

The C64x DSP applications can be observed in many common use devices such as sound devices, digital cameras, voice codec, wireless etc. For the available lists of drivers of devices based on C64x, visit http://focus.ti.com/dsp/docs/dspsupporta.tsp?sectionId=3&tabId=425&familyId=44&toolTypeId=32.
References

Documents
Taxes Instruments, Feb 2001, TMS320C6414, TMS320C6415, TMS320C6416
Fixed-Point Digital Signal Processor, Revised May 2005.


Web Links
http://www.ti.com
http://focus.ti.com
http://dsp.ti.com
http://en.wikipedia.com
http://whatis.techtarget.com
http://www.microcontroller.com
http://google.com
Appendix

Enhanced Direct Memory Access (EDMA) Controller

64 independent channels support various system dataflows

Facilitates sophisticated transfers in background of CPU - Auto initializing, linking, chaining of channels

2.4 GB/s sustained bandwidth

Unsurpassed efficiency and concurrency with the ability to automatically interleave traffic from multiple peripherals every cycle

Peripheral Component Interconnect (PCI)

C6415 and C6416 DSPs:

32-bit/33 MHz, 3.3V Master/Slave Interface Conforms to PCI Specification 2.1

Meets Requirements of PC99

Access to Entire Memory Map

Three PCI Bus Address Registers

Prefetchable Memory
Non-Prefetchable Memory I/O

Four-Wire Serial EEPROM Interface

PCI Interrupt Request Under DSP Program Control

DSP Interrupt Via PCI I/O Cycle
Universal Test and Operation PHY Interface for ATM (UTOPIA)

Utopia Level 2 ATM controller- C6415/C6416

8-bit Transmit and Receive Operations up to 50 MHz

User-defined cell format up to 64 bytes

Viterbi Coprocessor (VCP) - Applies to C6416 DSP only

Supports > 500 voice channels at 8 Kbps

Programmable decoder parameters include constraint length, code rate, and frame length

Turbo Coprocessor (TCP) - Applies to C6416 DSP only

Supports 35 data channels at 384 kbps

3GPP/IS2000 Turbo coder

Minimal processor delay

Programmable parameters include mode, rate and frame length

External Memory Interfaces (EMIFs)

Other densely integrated on-chip peripherals common to various C6000™ DSPs include:

Supports a glueless interface to several external devices including:

Synchronous burst SRAM (SBSRAM)
Synchronous DRAM (SDRAM)
Asynchronous devices including SRAM, ROM and FIFOs
An external shared-memory device
C6414/C6415/C6416 DSPs Provide Dual 133 MHz EMIFs

64-bit Interface for intended as a dedicated high speed interface to high performance industry standard memories
16-bit Interface for intended as a dedicated high speed interface to high performance industry standard memories
All other devices have a single 32-bit EMIF

Multi-channel Buffered Serial Ports (McBSPs)

High-speed full-duplex serial ports
Full-Duplex communication
Double-buffered data registers for continuous data stream
Direct interface to
C6000 devices
Industry-standard codecs, analog interface chips (AICs), and other serially connected A/D and D/A devices
ST-BUS compliant devices supporting
T1/E1 framers
H.110/H.100 Framers
MVIP and SCSA interface device
IOM-2 compliant devices
AC97 compliant devices
IIS compliant devices
SPI™ devices
Transmits and receives up to 128 channels
Select from 8-, 12-, 16-, 20-, 24-, or 32-bit data size
The C64x McBSPs support independent selection of up to 128 transmit and 128 receive channels
The C62x/C67x McBSPs support independent selection of up to 32 transmit and 32 receive channels
Highly programmable internal clock & frame generation

On-chip companding (COMpress & exPAND) hardware for data compression/expansion in either µ-law or A-law format

**Host Port Interfaces (HPI)**

32/16-bit HPI on C6414/C6415/C6416

16-bit HPI on C6201/C6211

Parallel port for host processor to directly access DSP’s memory space

The host device has ease of access because it is the master of the interface

Host & DSP can exchange information via internal/external memory

The host has direct access to memory-mapped peripherals

**Direct Memory Access (DMA) Controller**

Applies to C6201, C6202, C6203, C6204, C6205 DSPs only

Transfers data between points in the memory space without CPU intervention

Allows data movements to/from internal memory, external memory and peripherals to occur in background of CPU operation

Operates independent of CPU

Four programmable channels and a fifth auxiliary channel

Enhanced DMA (EDMA) has 16 programmable channels as well as a RAM space to hold multiple configurations for future transfers (C6x1x devices only)
32-bit Expansion Bus ("X-Bus")

Replaces the HPI on C6202, C6203 and C6204

Expansion Bus host port can operate in either asynchronous slave mode (similar to HPI) or in synchronous master/slave mode

Synchronous FIFOs and asynchronous peripheral I/O devices may interface to the Expansion Bus

**Serial RapidIO™**

Offers Increased Bandwidth for HD Video and Telecom Infrastructure Systems

Serial RapidIO is a high-performance, packet-switched, interconnect technology that addresses the embedded industry's need for:

- **Reliability**
- **Increased Bandwidth**
- **Faster Bus Speeds**

Serial RapidIO allows chip-to-chip and board-to-board communications at performance levels scaling to 25 Gigabits per second and beyond.

The C6455 DSP’s integrated Serial RapidIO™ (SRIO) bus decreases overall system cost by reducing the need for additional devices used for switching and processor aggregation. Supported by an industry association of leading device, system and software manufacturers, the SRIO interconnect enables high-speed, packet-switched peer-to-peer connectivity. SRIO thus makes it much easier to implement multi-processing, providing a performance breakthrough for multi-channel implementations on multiple processors.

For video infrastructure applications, a 1x SRIO link is fast enough to send high-definition (HD) 1080i raw video between devices and a 4x SRIO link can easily send HD 1080p raw video between devices with room to spare. The use of SRIO in infrastructure applications with large "DSP farms" will allow the reduction of system cost (device count, board size and/or device cost) for OEM customers.

**Serial RapidIO™ Enables Scalable DSP-Based Systems with Flexible Topologies**
Reduce System Cost with Serial Rapid IO™
These are the many ways video infrastructure, telecom infrastructure and medical/imaging customers can reduce system cost by arranging scalable systems with Serial Rapid IO (SRIO).

SRIO is very flexible - it can be arranged in a ring and mesh topologies. Or, multiple C6455 DSPs can be connected through a switch, with or without local connections to one another and to ASICs and FPGAs. You can also connect multiple C6455 DSPs in a star topology, where five DSPs are all connected to one another. The use of Serial RapidIO in applications with large "DSP farms" will allow the reduction of system cost for OEM customers.