SYStematic design of 3D Multicore Architectures with NeTwork-on-chIp Communication

Key Innovation
The widening gap between power and performance requirements of applications and what is afforded by technology scaling and architectural techniques, clearly points to multi-processor architectures as the solution. However, the traditional bus-based, shared memory computer architecture is not suitable for contemporary memory-demanding multiprocessor embedded applications, leading to a new interconnect paradigm, the emergence of Network-on-Chip (NoC) platforms.

The objective of the SYSMANTIC project is the development of an efficient and robust framework for the design of application-specific heterogeneous multicore architectures with NoC interconnect and their realization in 3-Dimensional (3D) platforms.

Technical Approach
Specifically, the project addresses three main open problems: 1) selecting the optimal heterogeneous multicore architecture for a target application, 2) mapping the selected MPSoC architecture to 3D platforms efficiently and 3) meeting strict performance, power and time-to-market constraints for such complex systems. SYSMANTIC addresses these challenges by developing new design flows and tools. In particular, there are four key innovations.

The first is the development of a high-level (C++/SystemC) framework for evaluating various heterogeneous NoC architecture parameters (available resources, NoC topologies, protocols, quality of service, etc), for the target application in terms of metrics such as performance, area, power consumption and heat distribution, and ultimately selecting the optimal one.

The second key innovation is the development of an automatic synthesizable HDL generation tool for the optimized architecture parameters determined by the high-level exploration framework for the target application domain, shortening the long and error-prone RTL design process, and use off-the-shelf components for rapid prototyping and verification/evaluation of the optimized NoC architecture.

The third key innovation is the implementation of the optimized architecture in 3D IC technology using the automatically generated HDL and by extending commercial IC design tools.

The final SYSMANTIC innovation is the integration of the above into a seamless systematic design flow.

Project partners	Country
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